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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/666,054	09/20/2000	Sang Ho Lee	HI-017	5515

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EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/666,054	LEE, SANG HO	
	Examiner	Art Unit	
	Andrew W Wahba	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7-12,14-17,19,20,22-27,29,31-35 and 37-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4 and 7-9* is/are allowed.

6)☒ Claim(s) *1-3,5,10-12,14,15,17,19,20,22-27,29,31-35 and 37-42* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

PHIRIN SAM
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-5, 7-12, 14-17, 19, 20, 22-27, 29, 31-35, 37-42 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 5, 17, 19, 22, 25, 34, 35, 37, 38, 39, and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by (Uriu et al, hereinafter "Uriu", US Patent 5,301,184). Uriu discloses a control system for switching duplicated switch units in an ATM exchange.

With regard to claim 1, Uriu discloses a first system including switch 21a (first board) is operating as the active system (active) and the second system including the switch 21b (second board) is operating as the standby system (standby) (column 5, lines 26-39). Uriu discloses monitor unit 26a (monitoring state information) that sets the active system indication bits in the VPI/VCI table 25a (column 5, lines 64-67). Similarly, the monitor unit 26b (monitoring state information) refers to the ATM header including the active system indication bit (determining an active or standby state), of each ATM

cell stored in buffer 23b and compares the read ATM header with the contents of VPI/VCI table 25b (column 6, lines 1-5). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system (switching the duplexing / transfer an active authority), the active system information bit "0" is written in each ATM cell applied to switch 21a and the active system indication bit "1" is written (generating information / update information) into each ATM cell (ATM cell information) applied to switch 21b (column 6, lines 16-23). The VPI/VCI table 25b stores a plurality of pairs of VPI/VCI (virtual path / virtual channel) relating to the ATM cells transferred via the second system (column 6, lines 5-7). Accordingly, a virtual path of 0 and a virtual channel of 0 would be stored.

With regard to claim 3, when the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system (conversion between the active and the standby state), the active system information bit "0" is written in each ATM cell applied to switch 21a (each board) and the active system indication bit "1" is written into each ATM cell applied to switch 21b (each board) (column 6, lines 16-23).

With regard to claim 5, the VPI/VCI table 25b stores a plurality of pairs of VPI/VCI (virtual path / virtual channel) relating to the ATM cells transferred via the second system (column 6, lines 5-7). Accordingly, a virtual path of 0 or 1 and a virtual channel of 255 would be stored.

With regard to claim 17, Uriu discloses a first system including switch 21a (first board) is operating as the active system (master) and the second system including the switch 21b (second board) is operating as the standby system (slave) (column 5, lines 26-39).

With regard to claim 19, when the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system (assume the active state), the active system information bit (state information) "0" is written in each ATM cell applied to switch 21a and the active system indication bit (state information) "1" is written into each ATM cell applied to switch 21b (column 6, lines 16-23).

With regard to claim 22, Uriu discloses a first system including switch 21a (first) is operating as the active system and the second system including the switch 21b (second) is operating as the standby system (column 5, lines 26-39). Uriu discloses monitor unit 26a (recognizing state information) that sets the active system indication bits in the VPI/VCI table 25a (column 5, lines 64-67). Similarly, the monitor unit 26b (recognizing state information) refers to the ATM header including the active system indication bit, of each ATM cell stored in buffer 23b and compares the read ATM header with the contents of VPI/VCI table 25b (column 6, lines 1-5). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system (switching the active authority / transfer an active authority), the active system information bit (state information) "0" is written (transfer command) in each ATM cell applied to switch 21a and the active

system indication bit (state information) "1" is written (transfer command / updating) into each ATM cell (ATM cell information) applied to switch 21b (column 6, lines 16-23)4. The VPI/VCI table 25b stores a plurality of pairs of VPI/VCI (virtual path / virtual channel) relating to the ATM cells transferred via the second system (column 6, lines 5-7). Accordingly, a virtual path of 0 and a virtual channel of 0 would be stored.

With regard to claim 25, Uriu discloses a first system including switch 21a (first) is operating as the active system (master) and the second system including the switch 21b (second) is operating as the standby system (slave) (column 5, lines 26-39). Uriu discloses monitor unit 26a (recognizing state information) that sets the active system indication bits in the VPI/VCI table 25a (column 5, lines 64-67). Similarly, the monitor unit 26b (recognizing state information) refers to the ATM header including the active system indication bit (determining), of each ATM cell stored in buffer 23b and compares the read ATM header with the contents of VPI/VCI table 25b (column 6, lines 1-5). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system (switching the duplexing / transfer an active authority), the active system information bit (generating information) "0" is written (generating information / recognized state information) in each ATM cell applied to switch 21a and the active system indication bit (generating information) "1" is written (updating) into each ATM cell applied to switch 21b (column 6, lines 16-23). The VPI/VCI table 25b stores a plurality of pairs of VPI/VCI (virtual path / virtual channel) relating to the ATM cells transferred via the second system (column 6, lines 5-7). Accordingly, a virtual path of 0 and a virtual channel of 0 would be stored.

With regard to claim 34, Uriu discloses a first system including switch 21a is operating as the active system and the second system including the switch 21b is operating as the standby system (column 5, lines 26-39). Figure 3 illustrates the components of both the active and the second system. Specifically, the each system comprises a switch 21a and 21b (at least one port), a demultiplexer 22a and 22b, a first buffer 23a and 23b (memory), a second buffer 24a and 24b (memory), a VPI/VCI table 25a and 25b (memory), and a monitor unit 26a and 26b (controller) (column 5, lines 14-26). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system (switching a duplexing), the active system information bit (state information) "0" is written in each ATM cell applied to switch 21a and the active system indication bit (state information) "1" is written into each ATM cell applied to switch 21b (column 6, lines 16-23). The monitor unit 26a changes the active system indication bit related to first ATM cell stored in the VPI/VCI table 25a. The second buffer 24a refers to the contents of VPI/VCI table 25a and prevents the first ATM cell from being written therein (column 6, lines 36-41).

With regard to claim 35, With regard to claim 34, Uriu discloses a first system including switch 21a is operating as the active system (active state) and the second system including the switch 21b is operating as the standby system (standby state) (column 5, lines 26-39).

With regard to claim 37, when the first system is switched from the active system to the standby system and the second system is switched from the standby system to

the active system, the active system information bit "0" is written in each ATM cell applied to switch 21a and the active system indication bit "1" is written into each ATM cell applied to switch 21b (column 6, lines 16-23). The writing of the active system information bit reads on applicant's reset signal. Uriu further discloses a multiplexer or selector 27 connected to buffers 24a and 24b (port switching active authority) (column 5, lines 25-29).

With regard to claim 38, Uriu discloses a transmission line interface (interface) (column 5, lines 27-28).

With regard to claim 39, Uriu discloses a first system including switch 21a is operating as the active system (master board) and the second system including the switch 21b is operating as the standby system (slave board) (column 5, lines 26-39). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system, the active system information bit (state information / storing state information) "0" is written in each ATM cell applied to switch 21a (receiving state information) and the active system indication bit (state information / storing state information) "1" is written into each ATM cell applied to switch 21b (receiving state information) (column 6, lines 16-23). The monitor unit 26a changes the active system indication bit related to first ATM cell stored in the VPI/VCI table 25a (virtual path / virtual channel) (column 6, lines.36-39).

With regard to claim 40, Uriu discloses a first system including switch 21a is operating as the active system (active state) and the second system including the switch 21b is operating as the standby system (standby state) (column 5, lines 26-39).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2, 10, 11, 12, 13, 14, 20, 23, 24, 26, 27, 29, 31, 32, 33, 41, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over (Uriu et al, hereinafter "Uriu", US Patent 5,301,184) in view of (Matsurama et al, hereinafter "Matsurama", US Patent 6,269,077).

With regard to claims 2, 10 and 11, Uriu discloses a first system including switch 21a (first board) is operating as the active system (active) and the second system including the switch 21b (second board) is operating as the standby system (standby) (column 5, lines 26-39). Uriu discloses monitor unit 26a (monitoring state information) that sets the active system indication bits in the VPI/VCI table 25a (column 5, lines 64-67). Similarly, the monitor unit 26b (monitoring state information) refers to the ATM header including the active system indication bit (determining an active or standby state), of each ATM cell stored in buffer 23b and compares the read ATM header with the contents of VPI/VCI table 25b (column 6, lines 1-5). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system (switching the duplexing / transfer an active authority), the active system information bit "0" is written in each ATM

cell applied to switch 21a and the active system indication bit "1" is written (generating information / update information) into each ATM cell (ATM cell information) applied to switch 21b (column 6, lines 16-23).

Uriu does not disclose wherein a state of an MS port determines whether a board is the first board or the second board or wherein the second board is operated in the active state and informs the first board of its state through an ACTOWN port or a first board, which is not maintained in the active state, requests state information from the second board.

Matsumura et al discloses system-switching control units 21 and 31 in both the active and standby units that are connected (MS port / ACTOWN) to one another as illustrated by Figure 2 (column 5, lines 35-38). Matsumura et al further discloses that the system-switching control unit 21 or 31 performs control operation (whether a board is the first board or the second board / informs ... when master board is in standby state / request state information) at the time of system switching over from the active to the standby system (column 4, lines 57-59).

A person of ordinary skill in the art would have been motivated to employ Matsumura in Uriu to provide a duplicated ATM switch that maintains delay qualities of the involved cells (Matsumura, column 2, lines 17-22). At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Uriu and Matsumura (collectively "Uriu-Matsumura" so as to obtain the invention as specified in claims 2, 10 and 11.

With regard to claim 20, Uriu further discloses a multiplexer or selector 27 connected to buffers 24a and 24b (board is mounted) (column 5, lines 25-29).

With regard to claims 12, 13 and 14 Uriu discloses a first system including switch 21a is operating as the active system and the second system including the switch 21b is operating as the standby system (column 5, lines 26-39). Figure 3 illustrates the components of both the active and the second system. Specifically, the each system comprises a switch 21a and 21b (first interface circuit/A-bus), a demultiplexer 22a and 22b, a first buffer 23a and 23b (memory), a second buffer 24a and 24b (memory), a VPI/VCI table 25a and 25b (memory), and a monitor unit 26a and 26b (cell disassembling and assembling circuit / control circuit) (column 5, lines 14-26). Uriu further discloses a transmission line interface (second interface circuit/C-bus) (column 5, lines 27-28). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system, the active system information bit (state information / signal) "0" is written in each ATM cell applied to switch 21a and the active system indication bit (state information / signal) "1" is written into each ATM cell applied to switch 21b (column 6, lines 16-23). The monitor unit 26a changes the active system indication bit related to first ATM cell stored in the VPI/VCI table 25a (column 6, lines 36-39).

Uriu does not disclose a plurality of input / output ports coupled to the input / output bus to transmit / receive state information.

Matsumura et al discloses system-switching control units 21 and 31 in both the active and standby units that are connected (plurality of input / output ports) to one

another as illustrated by Figure 2 (column 5, lines 35-38). Matsumura et al further discloses that the system-switching control unit 21 or 31 performs control operation (transmit / receive state information) at the time of system switching over from the active to the standby system (column 4, lines 57-59).

A person of ordinary skill in the art would have been motivated to employ Matsumura in Uriu to provide a duplicated ATM switch that maintains delay qualities of the involved cells (Matsumura, column 2, lines 17-22). At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Uriu and Matsumura (collectively "Uriu-Matsumura" so as to obtain the invention as specified in claims 12, 13, and 14.

With regard to claims 23 and 24, Uriu discloses a first system including switch 21a is operating as the active system (active system) and the second system including the switch 21b is operating as the standby system (standby system) (column 5, lines 26-39). Figure 3 illustrates the components of both the active and the second system. Specifically, the each system comprises a switch 21a and 21b, a demultiplexer 22a and 22b, a first buffer 23a and 23b, a second buffer 24a and 24b, a VPI/VCI table 25a and 25b, and a monitor unit 26a and 26b (control circuit) (column 5, lines 14-26). Uriu further discloses a transmission line interface (interface) (column 5, lines 27-28). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system, the active system information bit (state information) "0" is written in each ATM cell applied to switch 21a and the active system indication bit (state information) "1" is written into each

ATM cell applied to switch 21b (column 6, lines 16-23). The monitor unit 26a changes the active system indication bit related to first ATM cell stored in the VPI/VCI table 25a (virtual path / virtual channel) (column 6, lines 36-39).

Uriu does not disclose a plurality of input/output ports coupled to the input/output bus to transmit state information of the duplexing control circuit, and receive state information from at least one other duplexing control circuit.

Matsumura et al discloses system-switching control units 21 and 31 in both the active and standby units that are connected (coupled) to one another as illustrated by Figure 2 (column 5, lines 35-38). Matsumura et al further discloses that the system-switching control unit 21 or 31 performs control operation (monitors state information of at least one other) at the time of system switching over from the active to the standby system (column 4, lines 57-59).

A person of ordinary skill in the art would have been motivated to employ Matsumura in Uriu to provide a duplicated ATM switch that maintains delay qualities of the involved cells (Matsumura, column 2, lines 17-22). At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Uriu and Matsumura (collectively "Uriu-Matsumura" so as to obtain the invention as specified in claims 23 and 24.

With regard to claim 26, Uriu discloses a first system including switch 21a is operating as the active system (master board) and the second system including the switch 21b is operating as the standby system (slave) (column 5, lines 26-39). Connections between individual components of the active system and the second

system, as illustrated by Figure 3, read on applicant's "at least one bus" (column 5, lines 14-26). Uriu further discloses a multiplexer or selector 27 connected to buffers 24a and 24b (connecting ports on master board and slave board) (column 5, lines 25-29). The monitor unit 26a changes the active system indication bit related to first ATM cell stored in the VPI/VCI table 25a (virtual path / virtual channel) (column 6, lines 36-39).

Uriu does not disclose wherein signal lines carry state information for switching duplexing between the two boards.

Matsumura et al discloses system-switching control units 21 and 31 in both the active and standby units that are connected to one another (signal lines) as illustrated by Figure 2 (column 5, lines 35-38). Matsumura et al further discloses that the system-switching control unit 21 or 31 performs control operation at the time of system switching over from the active to the standby system (column 4, lines 57-59).

A person of ordinary skill in the art would have been motivated to employ Matsumura in Uriu to provide a duplicated ATM switch that maintains delay qualities of the involved cells (Matsumura, column 2, lines 17-22). At the time the invention was made, therefore, it would have been obvious to one of ordinary skill in the art to which the invention pertains to combine Uriu and Matsumura (collectively "Uriu-Matsumura" so as to obtain the invention as specified in claim 26.

With regard to claim 27, Matsumura et al discloses system-switching control units 21 and 31 in both the active and standby units that are connected to one another (signal lines) as illustrated by Figure 2 (column 5, lines 35-38). As Figure 2 illustrates there are

2 connections (number of signal lines is more than 1) between system-switching control units 21 and 31.

With regard to claim 29, Uriu discloses when the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system, the active system information bit "0" is written in each ATM cell applied to switch 21a and the active system indication bit "1" is written into each ATM cell applied to switch 21b (column 6, lines 16-23). The writing of the active system information bit reads on applicant's reset signal.

With further regard to claim 29, Matsumura et al discloses a system switching control unit in both the active and standby units that are connected (connecting) to one another as illustrated by Figure 2 (column 5, lines 35-38). A signal that indicates a change in state is inherent and would read on applicant's reset signal.

With regard to claim 31 and 32, Uriu discloses a first system including switch 21a is operating as the active system and the second system including the switch 21b is operating as the standby system (column 5, lines 26-39). Figure 3 illustrates the components of both the active and the second system. Specifically, the each system comprises a switch 21a and 21b (at least one port), a demultiplexer 22a and 22b, a first buffer 23a and 23b (memory), a second buffer 24a and 24b (memory), a VPI/VCI table 25a and 25b (memory), and a monitor unit 26a and 26b (controller) (column 5, lines 14-26). When the first system is switched from the active system to the standby system and the second system is switched from the standby system to the active system the active system information bit (state information) "0" is written in each ATM cell applied

to switch 21a and the active system indication bit (state information) "1" is written into each ATM cell applied to switch 21b (column 6, lines 16-23). The monitor unit 26a changes (updates) the active system indication bit (controls duplexing state) related to first ATM cell stored in the VPI/VCI table 25a. The second buffer 24a refers to the contents of VPI/VCI table 25a and prevents the first ATM cell from being written therein (column 6, lines 36-41).

With regard to claim 33, Matsumura et al discloses system-switching control units 21 and 31 in both the active and standby units that are connected to one another (controller of slave monitors) as illustrated by Figure 2 (column 5, lines 35-38).

With regard to claims 41, Matsumura et al discloses system-switching control units 21 and 31 in both the active and standby units that are connected to one another (pin-to-pin connection between the master and slave boards) as illustrated by Figure 2 (column 5, lines 35-38).

With regard to claim 42, Matsumura et al discloses a system switching control unit in both the active and standby units that are connected (connecting) to one another as illustrated by Figure 2 (column 5, lines 35-38). A signal that indicates a change in state is inherent and would read on applicant's reset signal.

Allowable Subject Matter

6. Claims 4 and 7-9 are allowed. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew W Wahba whose telephone number is (571) 272-3081. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth N Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Respectfully Submitted,

Andrew Wahba AW
Patent Examiner
January 21, 2005

PHIRIN SAM
PRIMARY EXAMINER

Notice of References Cited	Application/Control No. 09/666,054	Applicant(s)/Patent Under Reexamination LEE, SANG HO	
	Examiner Andrew W Wahba	Art Unit 2661	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,301,184 A	04-1994	Uriu et al.	370/219
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.